19-3653; Rev 0; 4/05

EVALUATION KIT AVAILABLE

1.8V, 12-Bit, 250Msps ADC for Broadband Applications

MAX1215

General Description

The MAX1215 is a monolithic, 12-bit, 250Msps analog-to-digital converter (ADC) optimized for outstanding dynamic performance at high-IF frequencies up to 300MHz. The product operates with conversion rates up to 250Msps while consuming only 975mW.

At 250Msps and an input frequency up to 250MHz, the MAX1215 achieves a spurious-free dynamic range (SFDR) of 72.4dBc. Its excellent signal-to-noise ratio (SNR) of 66dB at 10MHz remains flat (within 2dB) for input tones up to 300MHz. This ADC yields an excellent low noise floor of -67.5dBFS, which makes it ideal for wideband applications such as cable-head end receivers and power-amplifier predistortion in cellular base-station transceivers.

The MAX1215 requires a single 1.8V supply. The analog input is designed for either differential or single-ended operation and can be AC- or DC-coupled. The ADC also features a selectable on-chip divide-by-2 clock circuit, which allows the user to apply clock frequencies as high as 340MHz. This helps to reduce the phase noise of the input clock source. A low-voltage differential signal (LVDS) sampling clock is recommended for best performance. The converter's digital outputs are LVDS compatible and the data format can be selected to be either two's complement or offset binary.

The MAX1215 is available in a 68-pin QFN package with exposed paddle (EP) and is specified over the industrial (-40°C to +85°C) temperature range.

See the *Pin-Compatible Versions* table for a complete selection of 8-bit, 10-bit, and 12-bit high-speed ADCs in this family.

Applications

Base-Station Power-Amplifier Linearization

Cable-Head End Receivers

Wireless and Wired Broadband Communication

Communications Test Equipment

Radar and Satellite Subsystems

Pin Configuration appears at end of data sheet.

Features

- **250Msps Conversion Rate**
- **Low Noise Floor of -67.5dBFS**
- **Excellent Low-Noise Characteristics**
  SNR = 65.5dB at f_{IN} = 100MHz
  SNR = 65dB at f_{IN} = 250MHz
- **Excellent Dynamic Range**
  SFDR = 70.7dBc at f_{IN} = 100MHz
  SFDR = 72.4dBc at f_{IN} = 250MHz
- **65.4dB NPR for f_{NOTCH} = 28.8MHz and a Noise Bandwidth of 50MHz**
- **Single 1.8V Supply**
- **1006mW Power Dissipation at f_{SAMPLE} = 250MHz and f_{IN} = 100MHz**
- **On-Chip Track-and-Hold Amplifier**
- **Internal 1.24V-Bandgap Reference**
- **On-Chip Selectable Divide-by-2 Clock Input**
- **LVDS Digital Outputs with Data Clock Output**
- **MAX1215 EV Kit Available**

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX1215EGK	-40°C to +85°C	68 QFN-EP*

**EP = Exposed paddle.*

Pin-Compatible Versions

PART	RESOLUTION (BITS)	SPEED GRADE (Msps)
MAX1121	8	250
MAX1122	10	170
MAX1123	10	210
MAX1124	10	250
MAX1213	12	170
MAX1214	12	210

1.8V, 12-Bit, 250Msps ADC for Broadband Applications

ABSOLUTE MAXIMUM RATINGS

AV_{CC} to AGND ..... -0.3V to +2.1V
OV_{CC} to OGND ..... -0.3V to +2.1V
AV_{CC} to OV_{CC} ..... -0.3V to +2.1V
AGND to OGND ..... -0.3V to +0.3V
INP, INN to AGND .....-0.3V to (AV_{CC} + 0.3V)
All Digital Inputs to AGND.....-0.3V to (AV_{CC} + 0.3V)
REFIO, REFADJ to AGND .....-0.3V to (AV_{CC} + 0.3V)
All Digital Outputs to OGND .....-0.3V to (OV_{CC} + 0.3V)
ESD on All Pins (Human Body Model) .....±2000V

Thermal Resistance
θ_{JC} .....0.8°C/W
θ_{JA}.....35°C/W
Operating Temperature Range .....-40°C to +85°C
Junction Temperature .....+150°C
Storage Temperature Range .....-60°C to +150°C
Maximum Current into Any Pin.....50mA
Lead Temperature (soldering,10s) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(AV_{CC} = OV_{CC} = 1.8V, AGND = OGND = 0, f_{SAMPLE} = 250MHz, differential sine-wave clock input drive, 0.1µF capacitor on REFIO, internal reference, digital output pins differential R_L = 100Ω ±1%, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DC ACCURACY						
Resolution			12			Bits
Integral Nonlinearity (Note 2)	INL	f_{IN} = 10MHz, T_A = +25°C	-2	±0.85	+2	LSB
Differential Nonlinearity (Note 2)	DNL	T_A = +25°C, no missing codes	-1	±0.5	+1	LSB
Transfer Curve Offset	V_{OS}	T_A = +25°C (Note 2)	-3.5		+3.5	mV
Offset Temperature Drift				40		µV/°C
ANALOG INPUTS (INP, INN)						
Full-Scale Input Voltage Range	V_{FS}	T_A = +25°C (Note 2)	1320	1454	1590	mV_{P-P}
Full-Scale Range Temperature Drift				130		ppm/°C
Common-Mode Input Range	V_{CM}	Internally self-biased		1.365 ±0.15		V
Input Capacitance	C_{IN}			2.5		pF
Differential Input Resistance	R_{IN}		3.0	4.2	6.3	kΩ
Full-Power Analog Bandwidth	FPBW			700		MHz
REFERENCE (REFIO, REFADJ)						
Reference Output Voltage	V_{REFIO}	T_A = +25°C, REFADJ = AGND	1.18	1.23	1.30	V
Reference Temperature Drift				90		ppm/°C
REFADJ Input High Voltage	V_{REFADJ}	Used to disable the internal reference	AV_{CC} - 0.3			V
SAMPLING CHARACTERISTICS						
Maximum Sampling Rate	f_{SAMPLE}		250			MHz
Minimum Sampling Rate	f_{SAMPLE}			20		MHz
Clock Duty Cycle		Set by clock-management circuit		40 to 60		%
Aperture Delay	t_{AD}	Figures 4, 11		620		ps
Aperture Jitter	t_{AJ}	Figure 11		0.2		ps_{RMS}

ELECTRICAL CHARACTERISTICS (continued)

(AV_{CC} = OV_{CC} = 1.8V, AGND = OGND = 0, f_{SAMPLE} = 250MHz, differential sine-wave clock input drive, 0.1µF capacitor on REFIO, internal reference, digital output pins differential R_L = 100Ω ±1%, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
CLOCK INPUTS (CLKP, CLKN)						
Differential Clock Input Amplitude		(Note 3)	200	500		mV_{P-P}
Clock Input Common-Mode Voltage Range		Internally self-biased		1.15 ±0.25		V
Clock Differential Input Resistance	R_{CLK}			11 ±25%		kΩ
Clock Differential Input Capacitance	C_{CLK}			5		pF
DYNAMIC CHARACTERISTICS (at -1dBFS)						
Signal-to-Noise Ratio	SNR	f_{IN} = 10MHz, T_A ≥ +25°C	63.5	66		dB
		f_{IN} = 100MHz, T_A ≥ +25°C	63.4	65.5		
		f_{IN} = 200MHz		65.5		
		f_{IN} = 250MHz		65		
Signal-to-Noise and Distortion	SINAD	f_{IN} = 10MHz, T_A ≥ +25°C	63.5	65.8		dB
		f_{IN} = 100MHz, T_A ≥ +25°C	62	64.3		
		f_{IN} = 200MHz		63.2		
		f_{IN} = 250MHz		64.2		
Spurious-Free Dynamic Range	SFDR	f_{IN} = 10MHz, T_A ≥ +25°C	70	84		dBc
		f_{IN} = 100MHz, T_A ≥ +25°C	67	70.7		
		f_{IN} = 200MHz		67.1		
		f_{IN} = 250MHz		72.4		
Worst Harmonics (HD2 or HD3)		f_{IN} = 10MHz, T_A ≥ +25°C		-87	-70	dBc
		f_{IN} = 100MHz, T_A ≥ +25°C		-70.7	-67	
		f_{IN} = 200MHz		-67.1		
		f_{IN} = 250MHz		-72.4		
Two-Tone Intermodulation Distortion	TTIMD	f_{IN1} = 99MHz at -7dBFS, f_{IN2} = 101MHz at -7dBFS		-79		dBc
Noise-Power Ratio	NPR	f_{NOTCH} = 28.8MHz ±1MHz, noise BW = 50MHz, A_{IN} = -9.1dBFS		65.4		dB
LVDS DIGITAL OUTPUTS (D0P/N–D11P/N, ORP/N)						
Differential Output Voltage	$\|V_{OD}\|$	R_L = 100Ω ±1%	250		400	mV
Output Offset Voltage	OV_{OS}	R_L = 100Ω ±1%	1.125		1.310	V

1.8V, 12-Bit, 250Msps ADC for Broadband Applications

ELECTRICAL CHARACTERISTICS (continued)

(AV_{CC} = OV_{CC} = 1.8V, AGND = OGND = 0, f_{SAMPLE} = 250MHz, differential sine-wave clock input drive, 0.1µF capacitor on REFIO, internal reference, digital output pins differential R_L = 100Ω ±1%, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
LVCMOS DIGITAL INPUTS (CLKDIV, $\overline{T}$/B)						
Digital Input-Voltage Low	V_{IL}				0.2 x AV_{CC}	V
Digital Input-Voltage High	V_{IH}		0.8 x AV_{CC}			V
TIMING CHARACTERISTICS						
CLK-to-Data Propagation Delay	t_{PDL}	Figure 4		1.75		ns
CLK-to-DCLK Propagation Delay	t_{CPDL}	Figure 4		3.87		ns
DCLK-to-Data Propagation Delay	t_{PDL} - t_{CPDL}	Figure 4 (Note 3)	1.66	2.12	2.48	ns
LVDS Output Rise Time	t_{RISE}	20% to 80%, C_L = 5pF		460		ps
LVDS Output Fall Time	t_{FALL}	20% to 80%, C_L = 5pF		460		ps
Output Data Pipeline Delay	$t_{LATENCY}$	Figure 4		11		Clock cycles
POWER REQUIREMENTS						
Analog Supply Voltage Range	AV_{CC}		1.70	1.80	1.90	V
Digital Supply Voltage Range	OV_{CC}		1.70	1.80	1.90	V
Analog Supply Current	I_{AVCC}	f_{IN} = 100MHz		495	555	mA
Digital Supply Current	I_{OVCC}	f_{IN} = 100MHz		64	75	mA
Analog Power Dissipation	P_{DISS}	f_{IN} = 100MHz		1006	1134	mW
Power-Supply Rejection Ratio (Note 3)	PSRR	Offset		1.8		mV/V
		Gain		1.5		%FS/V

Note 1: ≥+25°C guaranteed by production test, <+25°C guaranteed by design and characterization.

Note 2: Static linearity and offset parameters are based on the end-point fit method. The full-scale range (FSR) is defined as 4095 x slope of the line.

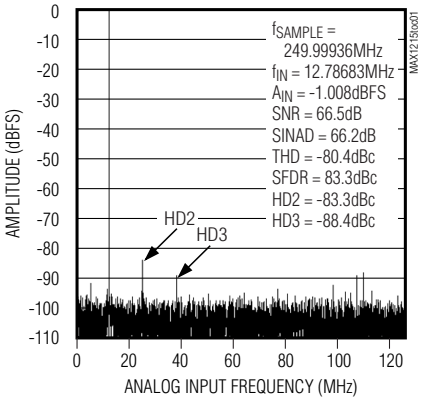
Note 3: Parameter guaranteed by design and characterization: T_A = T_{MIN} to T_{MAX}.

Note 4: PSRR is measured with both analog and digital supplies connected to the same potential.

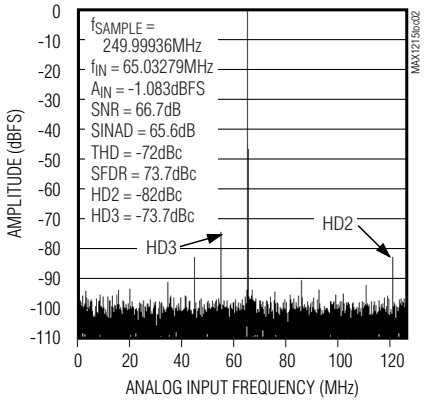
Typical Operating Characteristics

(AV_{CC} = OV_{CC} = 1.8V, AGND = OGND = 0, f_{SAMPLE} = 250MHz, A_{IN} = -1dBFS; see each TOC for detailed information on test conditions, differential input drive, differential sine-wave clock input drive, 0.1µF capacitor on REFIO, internal reference, digital output pins differential R_L = 100Ω, T_A = +25°C.)

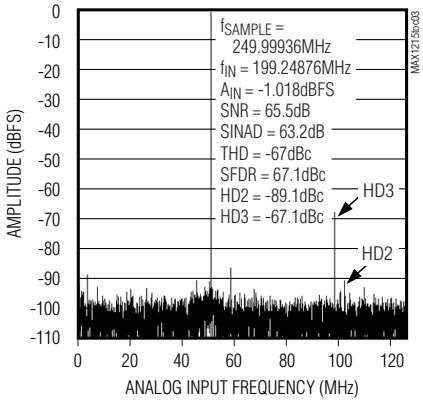
FFT PLOT (8192-POINT DATA RECORD)



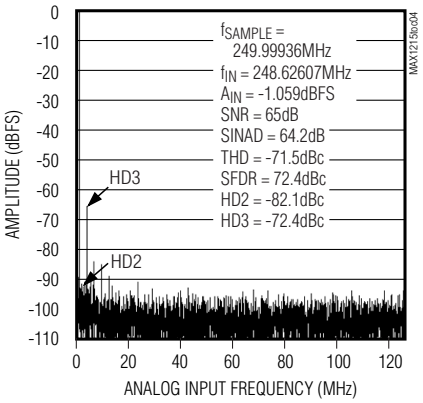
FFT PLOT (8192-POINT DATA RECORD)



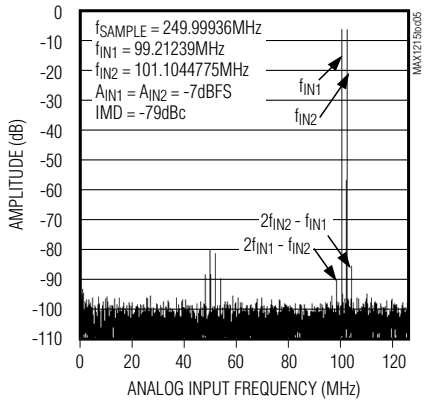
FFT PLOT (8192-POINT DATA RECORD)



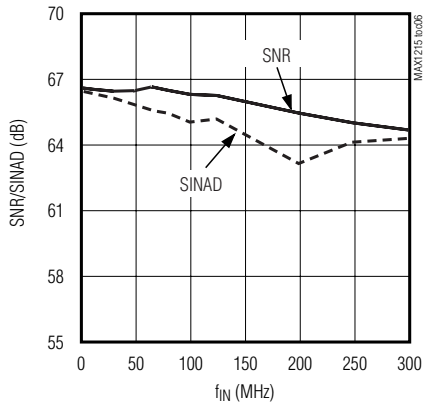
FFT PLOT (8192-POINT DATA RECORD)



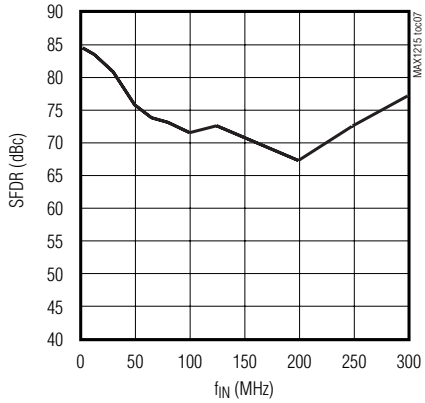
TWO-TONE IMD PLOT (8192-POINT DATA RECORD)



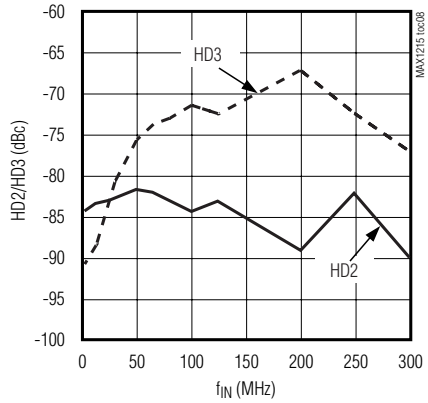
SNR/SINAD vs. ANALOG INPUT FREQUENCY (f_{SAMPLE} = 249.99936MHz, A_{IN} = -1dBFS)



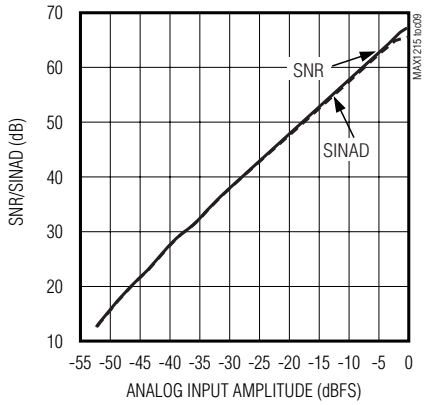
SFDR vs. ANALOG INPUT FREQUENCY (f_{SAMPLE} = 249.99936MHz, A_{IN} = -1dBFS)



HD2/HD3 vs. ANALOG INPUT FREQUENCY (f_{SAMPLE} = 249.99936MHz, A_{IN} = -1dBFS)



SNR/SINAD vs. ANALOG INPUT AMPLITUDE (f_{SAMPLE} = 249.99936MHz, f_{IN} = 65.03279MHz)

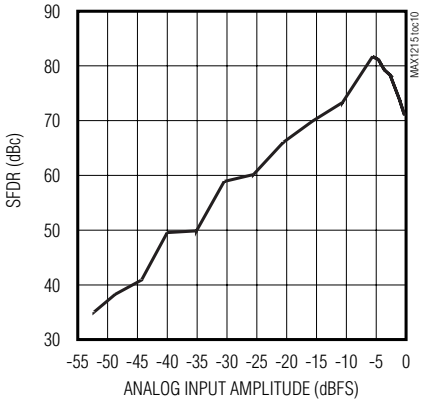


1.8V, 12-Bit, 250Msps ADC for Broadband Applications

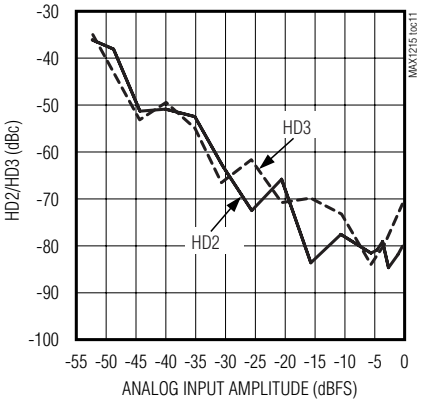
Typical Operating Characteristics (continued)

(AV_{CC} = OV_{CC} = 1.8V, AGND = OGND = 0, f_{SAMPLE} = 250MHz, A_{IN} = -1dBFS; see each TOC for detailed information on test conditions, differential input drive, differential sine-wave clock input drive, 0.1µF capacitor on REFIO, internal reference, digital output pins differential R_L = 100Ω, T_A = +25°C.)

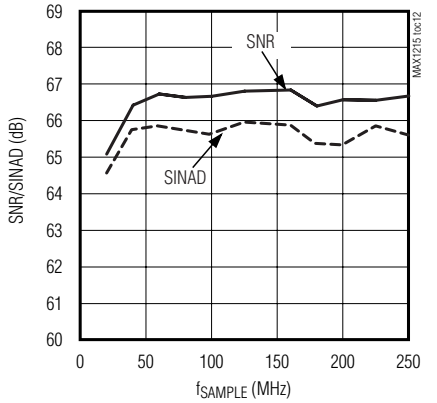
SFDR vs. ANALOG INPUT AMPLITUDE (f_{SAMPLE} = 249.99936MHz, f_{IN} = 65.03279MHz)



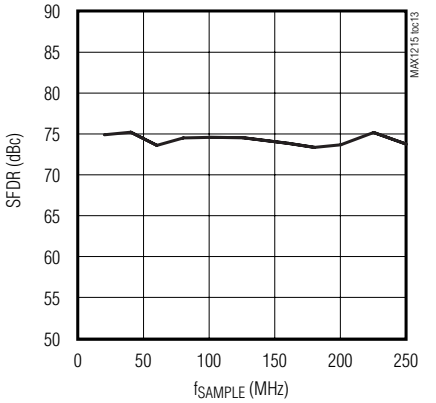
HD2/HD3 vs. ANALOG INPUT AMPLITUDE (f_{SAMPLE} = 249.99936MHz, f_{IN} = 65.03279MHz)



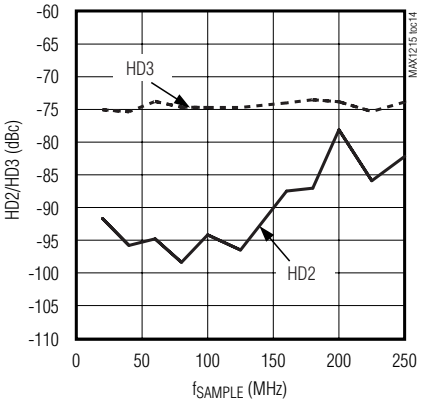
SNR/SINAD vs. SAMPLE FREQUENCY (f_{IN} = 65MHz, A_{IN} = -1dBFS)



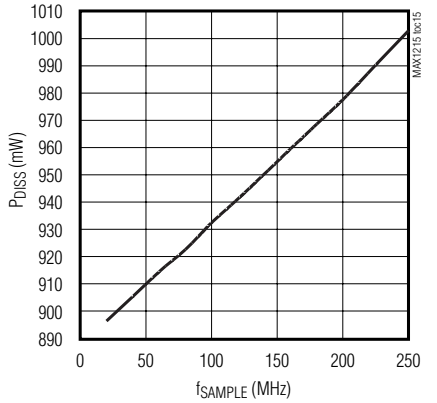
SFDR vs. SAMPLE FREQUENCY (f_{IN} = 65MHz, A_{IN} = -1dBFS)



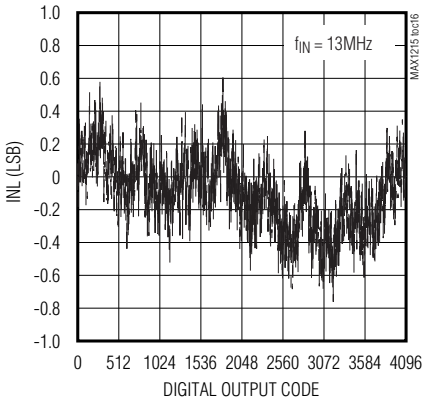
HD2/HD3 vs. SAMPLE FREQUENCY (f_{IN} = 65MHz, A_{IN} = -1dBFS)



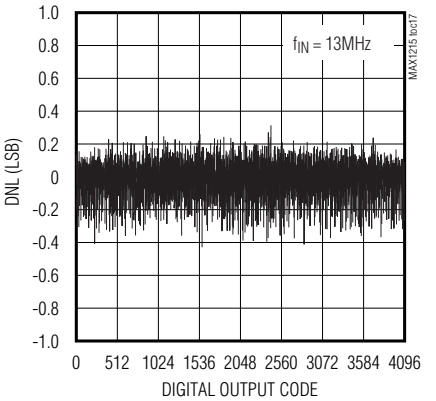
TOTAL POWER DISSIPATION vs. SAMPLE FREQUENCY (f_{IN} = 65MHz, A_{IN} = -1dBFS)



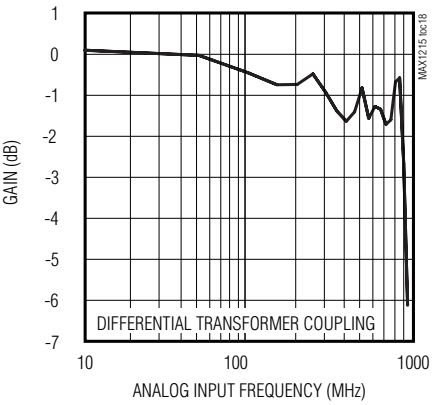
INTEGRAL NONLINEARITY vs. DIGITAL OUTPUT CODE



DIFFERENTIAL NONLINEARITY vs. DIGITAL OUTPUT CODE



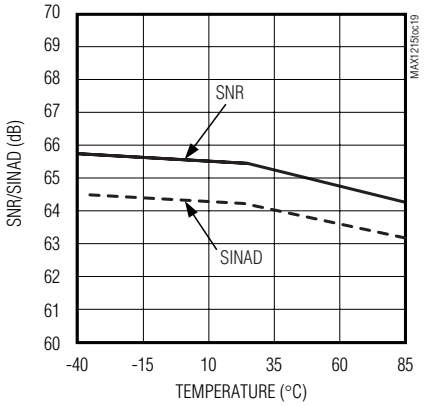
GAIN BANDWIDTH PLOT (f_{SAMPLE} = 249.99936MHz, A_{IN} = -1dBFS)



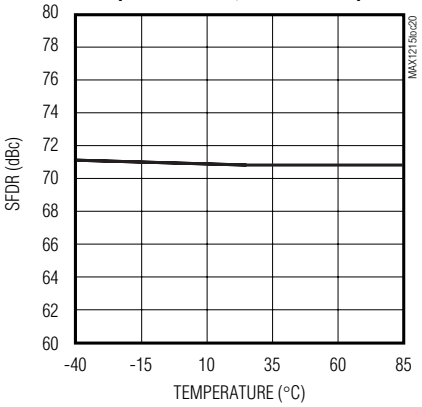
Typical Operating Characteristics (continued)

(AV_{CC} = OV_{CC} = 1.8V, AGND = OGND = 0, f_{SAMPLE} = 250MHz, A_{IN} = -1dBFS; see each TOC for detailed information on test conditions, differential input drive, differential sine-wave clock input drive, 0.1µF capacitor on REFIO, internal reference, digital output pins differential R_L = 100Ω, T_A = +25°C.)

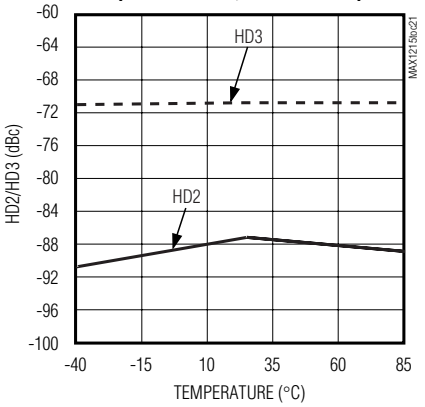
SNR/SINAD vs. TEMPERATURE (f_{IN} = 100MHz, A_{IN} = -1dBFS)



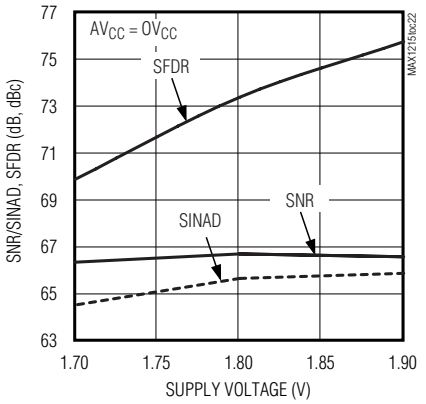
SFDR vs. TEMPERATURE (f_{IN} = 100MHz, A_{IN} = -1dBFS)



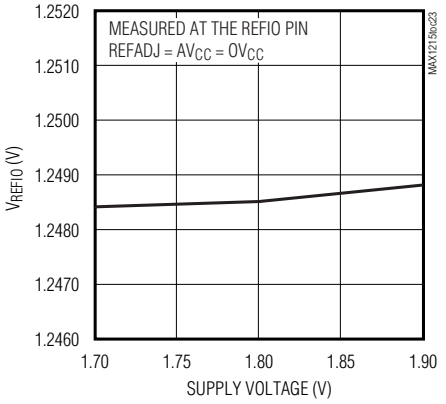
HD2/HD3 vs. TEMPERATURE (f_{IN} = 100MHz, A_{IN} = -1dBFS)



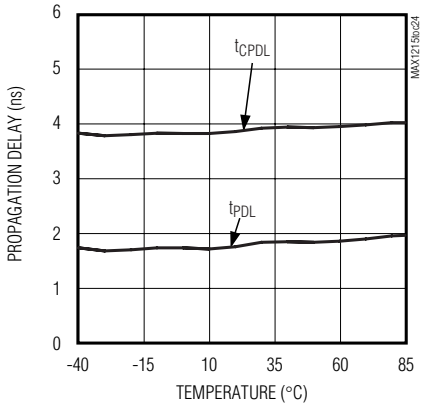
SNR/SINAD, SFDR vs. SUPPLY VOLTAGE (f_{IN} = 65.03279MHz, A_{IN} = -1dBFS)



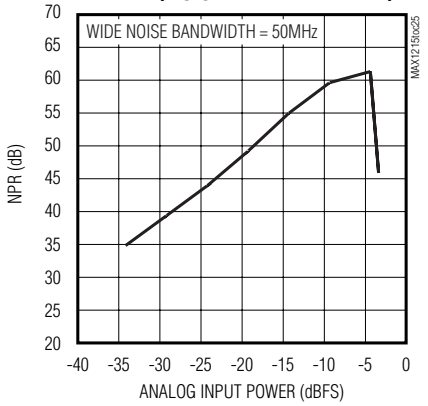
INTERNAL REFERENCE vs. SUPPLY VOLTAGE



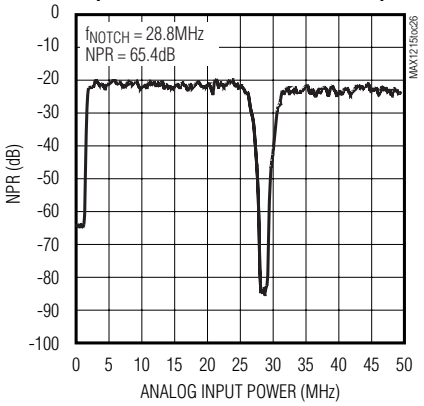
PROPAGATION DELAY TIMES vs. TEMPERATURE



NOISE-POWER RATIO vs. ANALOG INPUT POWER (f_{NOTCH} = 28.8MHz ± 1MHz)



NOISE-POWER RATIO PLOT (WIDE NOISE BANDWIDTH: 50MHz)



1.8V, 12-Bit, 250Msps ADC for Broadband Applications

Pin Description

PIN	NAME	FUNCTION
1, 6, 11–14, 20, 25, 62, 63, 65	AV_{CC}	Analog Supply Voltage. Bypass each pin with a parallel combination of 0.1µF and 0.22µF capacitors for best decoupling results.
2, 5, 7, 10, 15, 16, 18, 19, 21, 24, 64, 66, 67	AGND	Analog Converter Ground
3	REFIO	Reference Input/Output. With REFADJ pulled high, this I/O port allows an external reference source to be connected to the MAX1215. With REFADJ pulled low, the internal 1.23V bandgap reference is active.
4	REFADJ	Reference Adjust Input. REFADJ allows for FSR adjustments by placing a resistor or trim potentiometer between REFADJ and AGND (decreases FSR) or REFADJ and REFIO (increases FSR). If REFADJ is connected to AV_{CC}, the internal reference can be overdriven with an external source connected to REFIO. If REFADJ is connected to AGND, the internal reference is used to determine the FSR of the data converter.
8	INP	Positive Analog Input Terminal. Internally self-biased to 1.365V.
9	INN	Negative Analog Input Terminal. Internally self-biased to 1.365V.
17	CLKDIV	Clock Divider Input. This LVCMOS-compatible input controls with which speed the converter's digital outputs are updated. CLKDIV has an internal pulldown resistor. CLKDIV = 0: ADC updates digital outputs at one-half the input clock rate. CLKDIV = 1: ADC updates digital outputs at input clock rate.
22	CLKP	True Clock Input. This input ideally requires an LVPECL-compatible input level to maintain the converter's excellent performance. Internally self-biased to 1.15V.
23	CLKN	Complementary Clock Input. This input ideally requires an LVPECL-compatible input level to maintain the converter's excellent performance. Internally self-biased to 1.15V.
26, 45, 61	OGND	Digital Converter Ground. Ground connection for digital circuitry and output drivers.
27, 28, 41, 44, 60	OV_{CC}	Digital Supply Voltage. Bypass with a 0.1µF capacitor for best decoupling results.
29	D0N	Complementary Output Bit 0 (LSB)
30	D0P	True Output Bit 0 (LSB)
31	D1N	Complementary Output Bit 1
32	D1P	True Output Bit 1
33	D2N	Complementary Output Bit 2
34	D2P	True Output Bit 2
35	D3N	Complementary Output Bit 3
36	D3P	True Output Bit 3

Pin Description (continued)

PIN	NAME	FUNCTION
37	D4N	Complementary Output Bit 4
38	D4P	True Output Bit 4
39	D5N	Complementary Output Bit 5
40	D5P	True Output Bit 5
42	DCLKN	Complementary Clock Output. This output provides an LVDS-compatible output level and can be used to synchronize external devices to the converter clock.
43	DCLKP	True Clock Output. This output provides an LVDS-compatible output level and can be used to synchronize external devices to the converter clock.
46	D6N	Complementary Output Bit 6
47	D6P	True Output Bit 6
48	D7N	Complementary Output Bit 7
49	D7P	True Output Bit 7
50	D8N	Complementary Output Bit 8
51	D8P	True Output Bit 8
52	D9N	Complementary Output Bit 9
53	D9P	True Output Bit 9
54	D10N	Complementary Output Bit 10
55	D10P	True Output Bit 10
56	D11N	Complementary Output Bit 11 (MSB)
57	D11P	True Output Bit 11 (MSB)
58	ORN	Complementary Output for Out-of-Range Control Bit. If an out-of-range condition is detected, bit ORN flags this condition by transitioning low.
59	ORP	True Output for Out-of-Range Control Bit. If an out-of-range condition is detected, bit ORP flags this condition by transitioning high.
68	$\overline{T}$/B	Two's Complement or Binary Output Format Selection. This LVCMOS-compatible input controls the digital output format of the MAX1215. $\overline{T}$/B has an internal pulldown resistor. $\overline{T}$/B = 0: Two's complement output format. $\overline{T}$/B = 1: Binary output format.
—	EP	Exposed Paddle. The exposed paddle is located on the backside of the chip and must be connected to analog ground for optimum performance.

1.8V, 12-Bit, 250Msps ADC for Broadband Applications

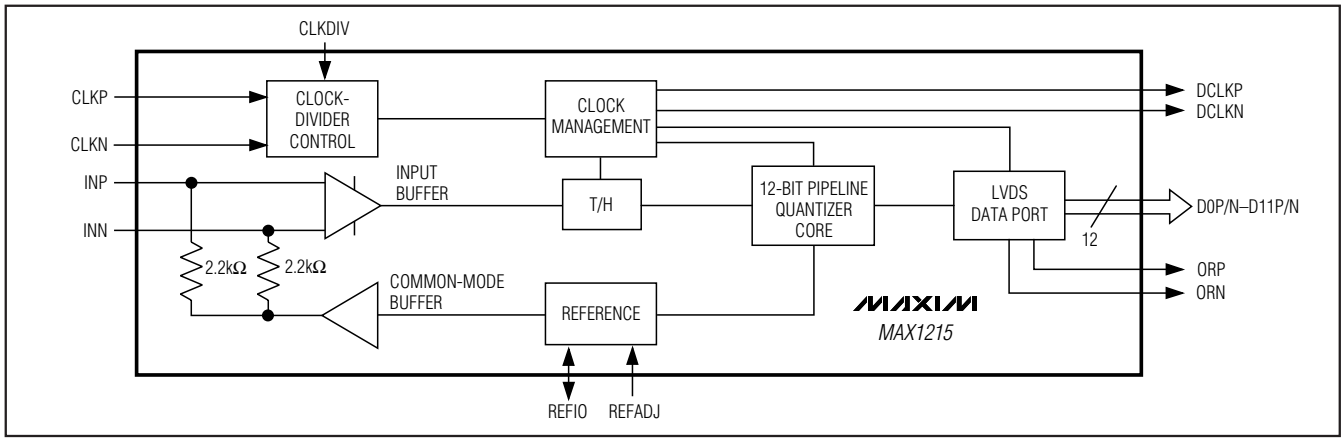


Figure 1. MAX1215 Block Diagram

Detailed Description—Theory of Operation

The MAX1215 uses a fully differential pipelined architecture that allows for high-speed conversion, optimized accuracy, and linearity while minimizing power consumption and die size.

Both positive (INP) and negative/complementary analog input terminals (INN) are centered around a 1.365V common-mode voltage, and accept a differential analog input voltage swing of $\pm V_{FS}$ / 4V each, resulting in a typical $1.454V_{P-P}$ differential full-scale signal swing. Inputs INP and INN are buffered prior to entering each T/H stage and are sampled when the differential sampling clock signal transitions high.

Each pipeline converter stage converts its input voltage to a digital output code. At every stage, except the last, the error between the input voltage and the digital output code is multiplied and passed along to the next pipeline stage. Digital error correction compensates for ADC comparator offsets in each pipeline stage and ensures no missing codes. The result is a 12-bit parallel digital output word in user-selectable two's-complement or offset binary output formats with LVDS-compatible output levels. See Figure 1 for a more detailed view of the MAX1215 architecture.

Analog Inputs (INP, INN)

INP and INN are the fully differential inputs of the MAX1215. Differential inputs usually feature good rejection of even-order harmonics, which allows for enhanced AC performance as the signals are progressing through the analog stages. The MAX1215 analog inputs are self-biased at a 1.365V common-mode voltage and allow a $1.454V_{P-P}$ differential input voltage swing (Figure 2). Both inputs are self-biased through

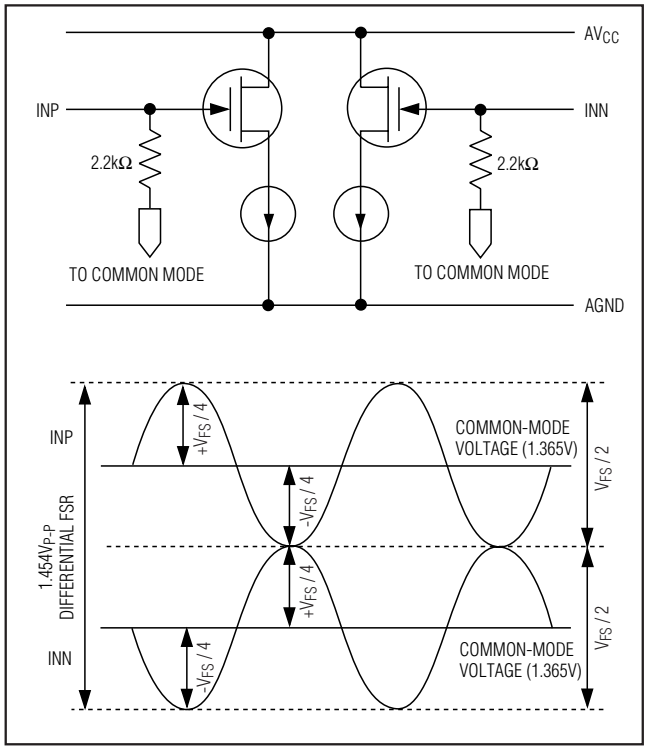


Figure 2. Simplified Analog Input Architecture and Allowable Input Voltage Range

2kΩ resistors, resulting in a typical differential input resistance of 4kΩ. It is recommended to drive the analog inputs of the MAX1215 in AC-coupled configuration to achieve best dynamic performance. See the *Transformer-Coupled, Differential Analog Input Drive* section for a detailed discussion of this configuration.

On-Chip Reference Circuit

The MAX1215 features an internal 1.23V bandgap reference circuit (Figure 3), which in combination with an internal reference-scaling amplifier determines the FSR of the MAX1215. Bypass REFIO with a 0.1µF capacitor to AGND. To compensate for gain errors or increase the ADC's FSR, the voltage of this bandgap reference can be indirectly adjusted by adding an external resistor (e.g., 100kΩ trim potentiometer) between REFADJ and AGND or REFADJ and REFIO. See the *Applications Information* section for a detailed description of this process.

To disable the internal reference, connect REFADJ to AV_{CC}. In this configuration, an external, stable reference must be applied to REFIO to set the converter's full scale. To enable the internal reference, connect REFADJ to AGND.

Clock Inputs (CLKP, CLKN)

Designed for a differential LVDS clock input drive, it is recommended to drive the clock inputs of the MAX1215 with an LVDS- or LVPECL-compatible clock to achieve the best dynamic performance. The clock signal source must be a high-quality, low phase noise with fast edge rates to avoid any degradation in the noise performance of the ADC. The clock inputs (CLKP, CLKN) are internally biased to 1.15V, accept a typical $0.5V_{P-P}$ differential signal swing, and are usually driven in AC-coupled configuration. See the *Differential, AC-Coupled PECL-Compatible Clock Input* section for more circuit details on how to drive CLKP and CLKN appropriately. Although not recommended, the clock inputs also accept a single-ended input signal.

The MAX1215 also features an internal clock-management circuit (duty-cycle equalizer) that ensures the clock signal applied to inputs CLKP and CLKN is processed to provide a 50% duty-cycle clock signal that desensitizes the performance of the converter to variations in the duty cycle of the input clock source. Note that the clock duty-cycle equalizer cannot be turned off externally and requires a minimum clock frequency of >20MHz to work appropriately and according to data sheet specifications.

Data Clock Outputs (DCLKP, DCLKN)

The MAX1215 features a differential clock output, which can be used to latch the digital output data with an external latch or receiver. Additionally, the clock output can be used to synchronize external devices (e.g., FPGAs) to the ADC. DCLKP and DCLKN are differential outputs with LVDS-compatible voltage levels. There is a 3.87ns delay time between the rising (falling) edge of CLKP (CLKN) and the rising edge of DCLKP (DCLKN). See Figure 4 for timing details.

Divide-by-2 Clock Control (CLKDIV)

The MAX1215 offers a clock control line (CLKDIV), which supports the reduction of clock jitter in a system. Connect CLKDIV to OGND to enable the ADC's internal divide-by-2 clock divider. Data is now updated at one-half the ADC's input clock rate. CLKDIV has an internal pulldown resistor and can be left open for applications that require this divide-by-2 mode. Connecting CLKDIV to OV_{CC} disables the divide-by-2 mode.

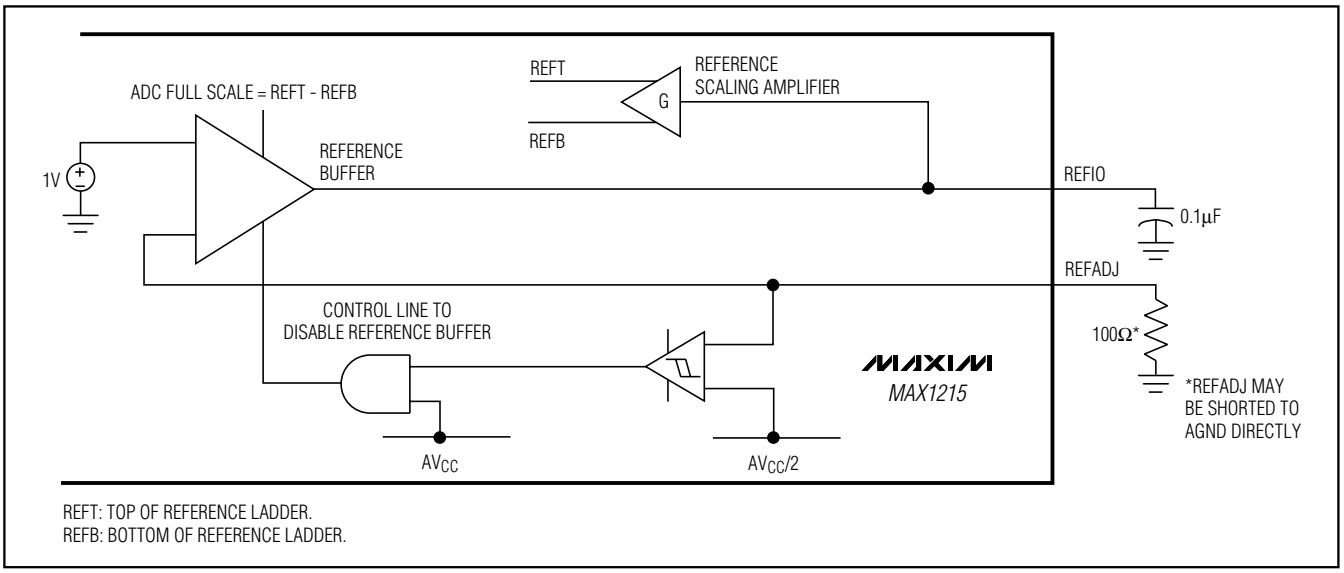


Figure 3. Simplified Reference Architecture

1.8V, 12-Bit, 250Msps ADC for Broadband Applications

System Timing Requirements

Figure 4 depicts the relationship between the clock input and output, analog input, sampling event, and data output. The MAX1215 samples on the rising (falling) edge of CLKP (CLKN). Output data is valid on the next rising (falling) edge of the DCLKP (DCLKN) clock, but has an internal latency of 11 clock cycles.

Digital Outputs (D0P/N–D11P/N, DCLKP/N, ORP/N) and Control Input $\overline{T}$/B

Digital outputs D0P/N–D11P/N, DCLKP/N, and ORP/N are LVDS compatible, and data on D0P/N–D11P/N is presented in either binary or two's-complement format (Table 1). The $\overline{T}$/B control line is an LVCMOS-compatible input, which allows the user to select the desired output format. Pulling $\overline{T}$/B low outputs data in two's complement and pulling it high presents data in offset binary format on the 12-bit parallel bus. $\overline{T}$/B has an internal pulldown resistor and may be left unconnected in applications using only two's-complement output format. All LVDS outputs provide a typical voltage swing of 0.325V around a common-mode voltage of roughly 1.15V, and must be terminated at the far end of each transmission line pair (true and complementary) with 100Ω. The LVDS outputs are powered from a separate power supply, which can be operated between 1.7V and 1.9V.

The MAX1215 offers an additional differential output pair (ORP, ORN) to flag out-of-range conditions, where out-of-range is above positive or below negative full scale. An out-of-range condition is identified with ORP (ORN) transitioning high (low).

Note: Although a differential LVDS output architecture reduces single-ended transients to the supply and ground planes, capacitive loading on the digital outputs should still be kept as low as possible. Using LVDS buffers on the digital outputs of the ADC when driving larger loads may improve overall performance and reduce system-timing constraints.

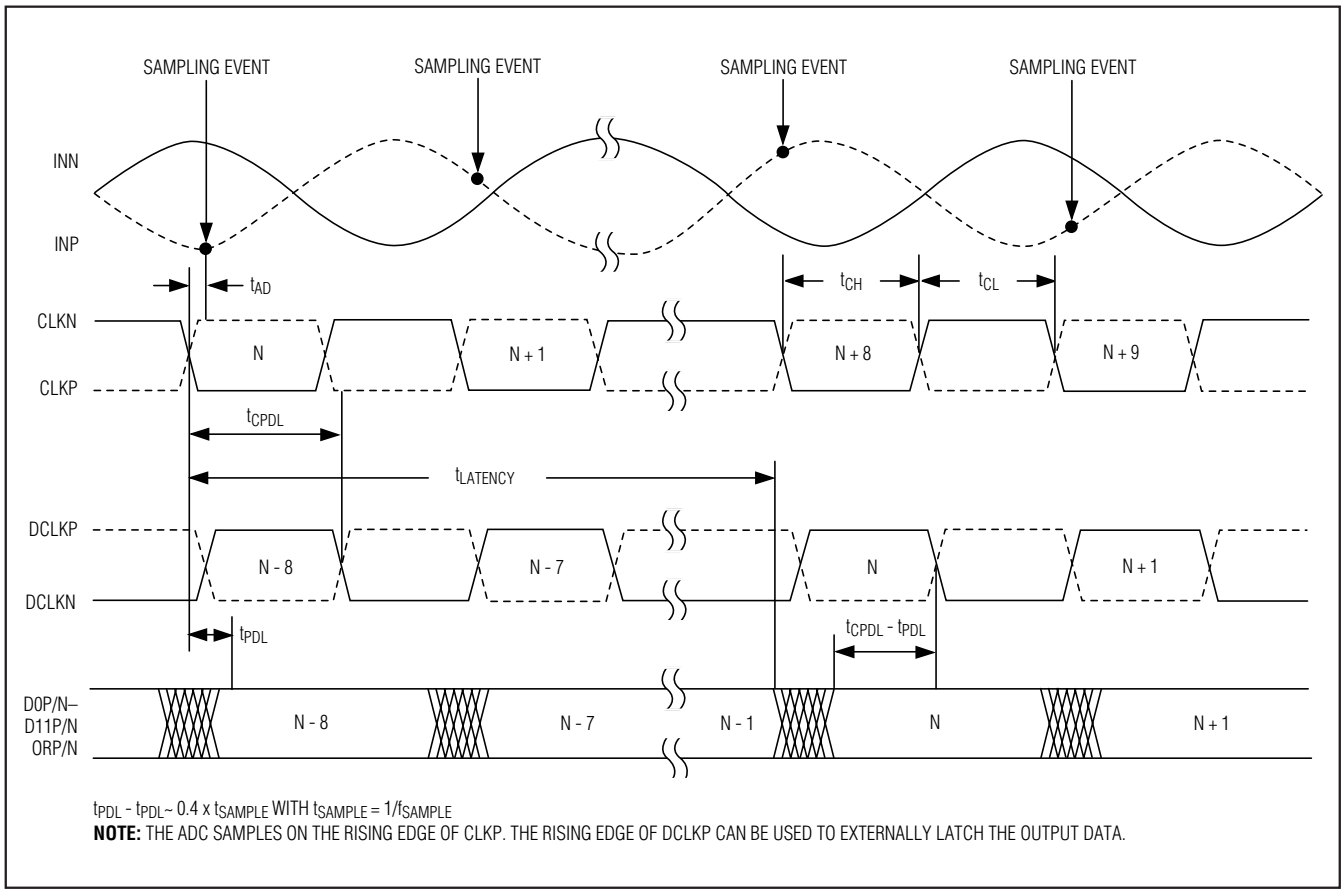


Figure 4. System and Output Timing Diagram

Table 1. MAX1215 Digital Output Coding

INP ANALOG INPUT VOLTAGE LEVEL	INN ANALOG INPUT VOLTAGE LEVEL	OUT-OF-RANGE ORP (ORN)	BINARY DIGITAL OUTPUT CODE (D11P/N–D0P/N)	TWO'S COMPLEMENT DIGITAL OUTPUT CODE (D11P/N–D0P/N)
> V_{CM} + V_{FS} / 4	< V_{CM} - V_{FS} / 4	1 (0)	1111 1111 1111 (exceeds +FS, OR set)	0111 1111 1111 (exceeds +FS, OR set)
V_{CM} + V_{FS} / 4	V_{CM} - V_{FS} / 4	0 (1)	1111 1111 1111 (+FS)	0111 1111 1111 (+FS)
V_{CM}	V_{CM}	0 (1)	1000 0000 0000 or 0111 1111 1111 (FS/2)	0000 0000 0000 or 1111 1111 1111 (FS/2)
V_{CM} - V_{FS} / 4	V_{CM} + V_{FS} / 4	0 (1)	0000 0000 0000 (-FS)	1000 0000 0000 (-FS)
< V_{CM} + V_{FS} / 4	> V_{CM} - V_{FS} / 4	1 (0)	00 0000 0000 (exceeds -FS, OR set)	10 0000 0000 (exceeds -FS, OR set)

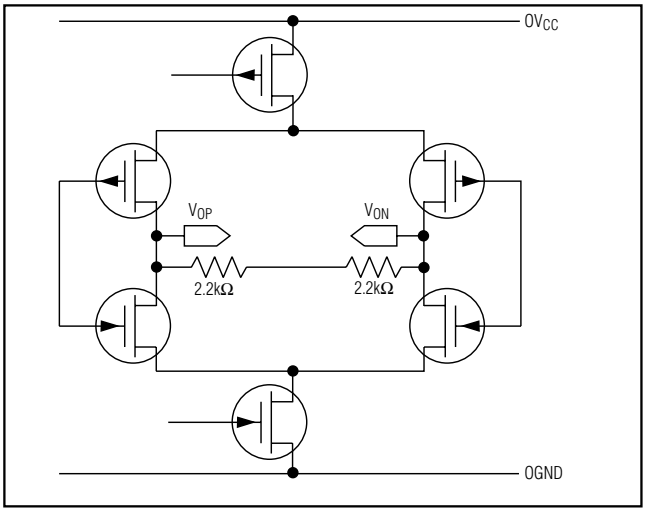


Figure 5. Simplified LVDS Output Architecture

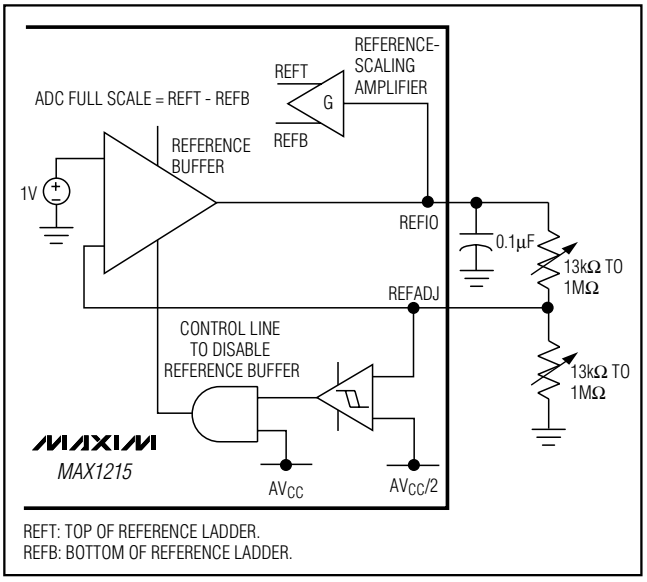


Figure 6a. Circuit Suggestions to Adjust the ADC's Full-Scale Range

Applications Information

FSR Adjustments Using the Internal Bandgap Reference

The MAX1215 supports a full-scale adjustment range of 10% (±5%). To decrease the full-scale signal range, an external resistor value ranging from 13kΩ to 1MΩ may be added between REFADJ and AGND. A similar approach can be taken to increase the ADC's full-scale range (FSR). Adding a variable resistor, potentiometer, or predetermined resistor value between REFADJ and REFIO increases the FSR of the data converter. Figure 6a shows the two possible configurations and their impact on the overall full-scale range adjustment of the MAX1215. Do not use resistor values of less than 13kΩ to avoid instability of the internal gain regulation loop for the bandgap reference. See Figure 6b for the results of the adjustment range for a selection of resistors used to trim the full-scale range of the MAX1215.

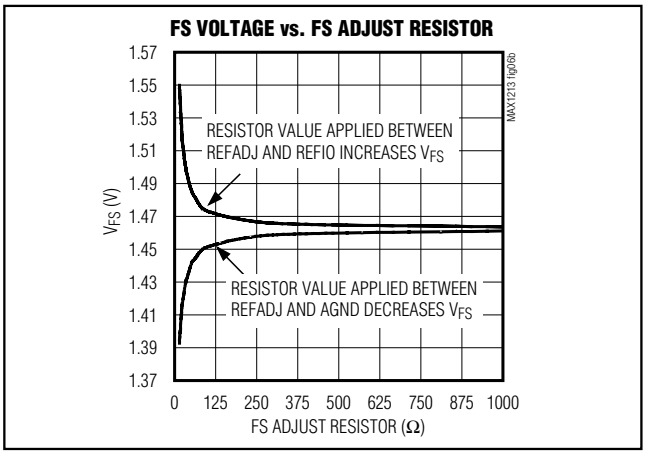


Figure 6b. FS Adjustment Range vs. FS Adjustment Resistor

1.8V, 12-Bit, 250Msps ADC for Broadband Applications

Differential, AC-Coupled, LVPECL-Compatible Clock Input

The MAX1215 dynamic performance depends on the use of a very clean clock source. The phase noise floor of the clock source has a negative impact on the SNR performance. Spurious signals on the clock signal source also affect the ADC's dynamic range. The preferred method of clocking the MAX1215 is differentially with LVDS- or LVPECL-compatible input levels. The fast data transition rates of these logic families minimize the clock input circuitry's transition uncertainty, thereby improving the SNR performance. To accomplish this, a 50Ω reverse-terminated clock signal source with low phase noise is AC-coupled into a fast differential receiver such as the MC100LVEL16D (Figure 7). The receiver produces the necessary LVPECL output levels to drive the clock inputs of the data converter.

Transformer-Coupled, Differential Analog Input Drive

In general, the MAX1215 provides the best SFDR and THD with fully differential input signals and it is not recommended to drive the ADC inputs in single-ended configuration. In differential input mode, even-order harmonics are usually lower since INP and INN are balanced, and each of the ADC inputs only requires half the signal swing compared to a single-ended configuration. Wideband RF transformers provide an excellent solution to convert a single-ended signal to a fully differential signal, required by the MAX1215 to reach its optimum dynamic performance.

A secondary-side termination of a 1:1 transformer (e.g., Mini-Circuit's ADT1-1WT) into two separate 24.9Ω ±1% resistors (use tight resistor tolerances to minimize effects of imbalance; 0.5% would be an ideal choice) placed between top/bottom and center tap of the transformer is recommended to maximize the ADC's dynamic range. This configuration optimizes THD and SFDR performance of the ADC by reducing the effects of transformer parasitics. However, the source impedance combined with the shunt capacitance provided by a PC board and the ADC's parasitic capacitance limit the ADC's full-power input bandwidth to approximately 600MHz.

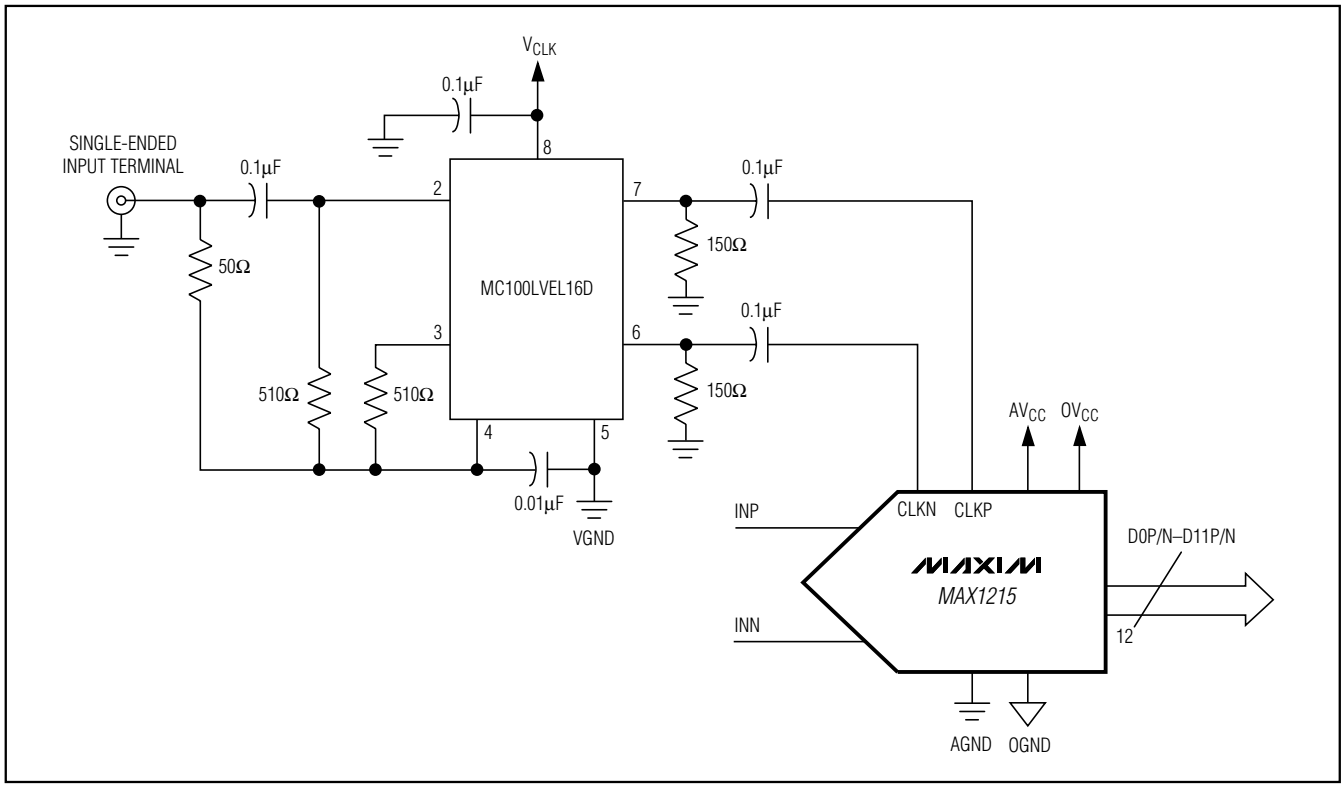


Figure 7. Differential, AC-Coupled, PECL-Compatible Clock Input Configuration

To further enhance THD and SFDR performance at high input frequencies (>100MHz), a second transformer (Figure 8) should be placed in series with the single-ended-to-differential conversion transformer. This transformer reduces the increase of even-order harmonics at high frequencies.

Single-Ended, AC-Coupled Analog Inputs

Although not recommended, the MAX1215 can be used in single-ended mode (Figure 9). Analog signals can be AC-coupled to the positive input INP through a 0.1µF capacitor and terminated with a 49.9Ω resistor to AGND. The negative input should be reverse terminated with 24.9Ω resistors and AC-grounded with a 0.1µF capacitor.

Grounding, Bypassing, and Board Layout Considerations

The MAX1215 requires board layout design techniques suitable for high-speed data converters. This ADC provides separate analog and digital power supplies. The analog and digital supply voltage pins accept 1.7V to 1.9V input voltage ranges. Although both supply types can be combined and supplied from one source, it is recommended to use separate sources to cut down on performance degradation caused by digital switching currents, which can couple into the analog supply network. Isolate analog and digital supplies (AV_{CC} and OV_{CC}) where they enter the PC board with separate networks of ferrite beads and capacitors to their corresponding grounds (AGND, OGND).

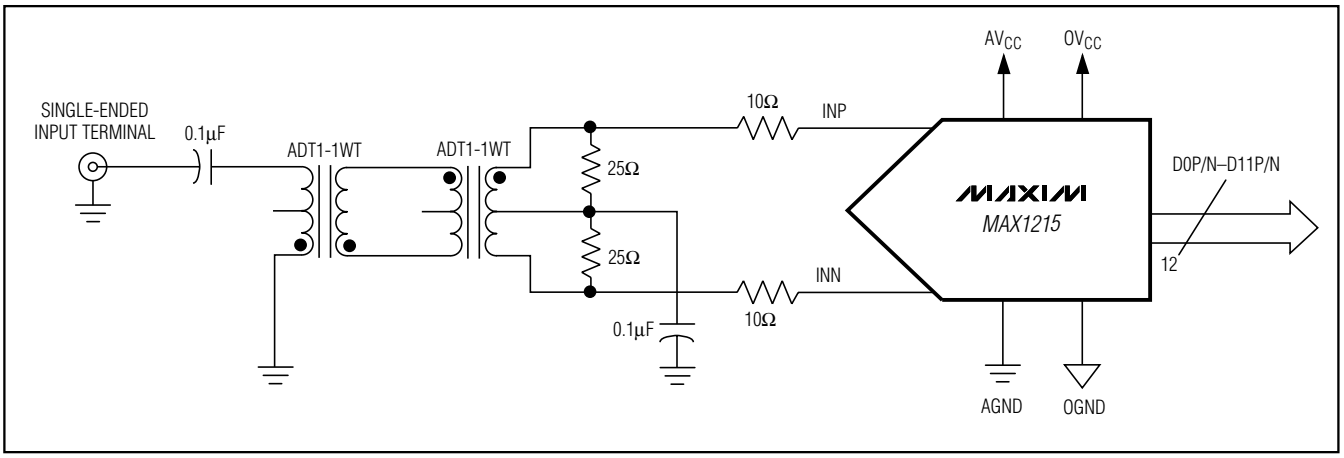


Figure 8. Analog Input Configuration with Back-to-Back Transformers and Secondary-Side Termination

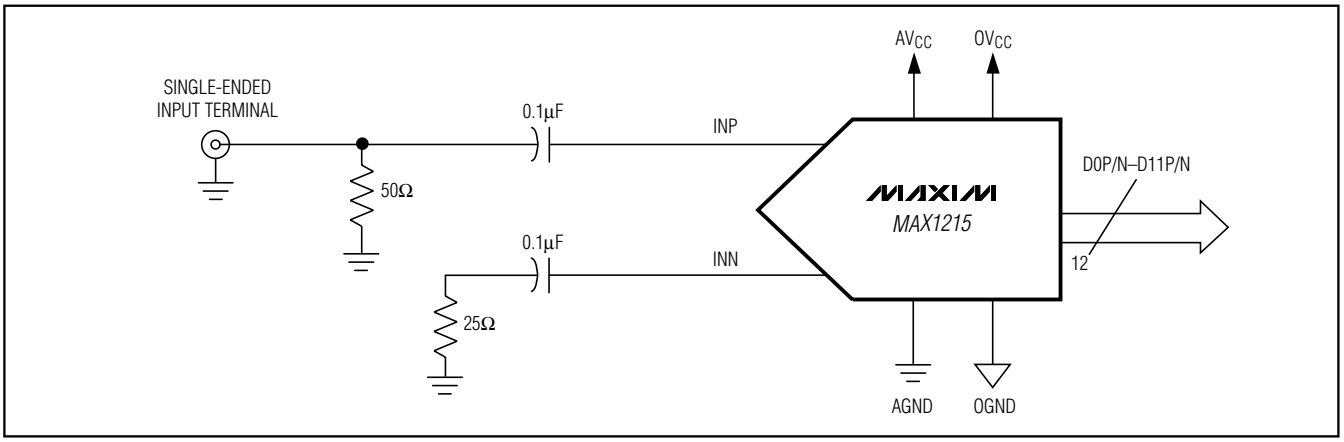


Figure 9. Single-Ended AC-Coupled Analog Input Configuration

1.8V, 12-Bit, 250Msps ADC for Broadband Applications

To achieve optimum performance, provide each supply with a separate network of a 47µF tantalum capacitor and parallel combinations of 10µF and 1µF ceramic capacitors. Additionally, the ADC requires each supply pin to be bypassed with separate 0.1µF ceramic capacitors (Figure 10). Locate these capacitors directly at the ADC supply pins or as close as possible to the MAX1215. Choose surface-mount capacitors, whose preferred location should be on the same side as the converter to save space and minimize the inductance. If close placement on the same side is not possible, these bypassing capacitors may be routed through vias to the bottom side of the PC board.

Multilayer boards with separated ground and power planes produce the highest level of signal integrity. Consider the use of a split ground plane arranged to match the physical location of analog and digital ground on the ADC's package. The two ground planes should be joined at a single point so the noisy digital ground currents do not interfere with the analog ground plane. The dynamic currents that may need to travel long distances before they are recombined at a common-source ground, resulting in large and undesirable ground loops, are a major concern with this approach. Ground loops can degrade the input noise by coupling back to the analog front-end of the converter, resulting in increased spurious activity, leading to decreased noise performance.

Alternatively, all ground pins could share the same ground plane, if the ground plane is sufficiently isolated from any noisy, digital systems ground. To minimize the coupling of the digital output signals from the analog input, segregate the digital output bus carefully from the analog input circuitry. To further minimize the effects of digital noise coupling, ground return vias can be positioned throughout the layout to divert digital switching currents away from the sensitive analog sections of the ADC. This approach does not require split ground planes, but can be accomplished by placing substantial ground connections between the analog front-end and the digital outputs.

The MAX1215 is packaged in a 68-pin QFN-EP package **(package code: G6800-4)**, providing greater design flexibility, increased thermal dissipation, and optimized AC performance of the ADC. The exposed paddle (EP) must be soldered down to AGND.

In this package, the data converter die is attached to an EP lead frame with the back of this frame exposed at the package bottom surface, facing the PC board side of the package. This allows a solid attachment of the package to the board with standard infrared (IR) flow soldering techniques.

Thermal efficiency is one of the factors for selecting a package with an exposed pad for the MAX1215. The exposed pad improves thermal and ensures a solid ground connection between the DAC and the PC board's analog ground layer.

Considerable care must be taken when routing the digital output traces for a high-speed, high-resolution data converter. It is recommended running the LVDS output traces as differential lines with 100Ω matched impedance from the ADC to the LVDS load device.

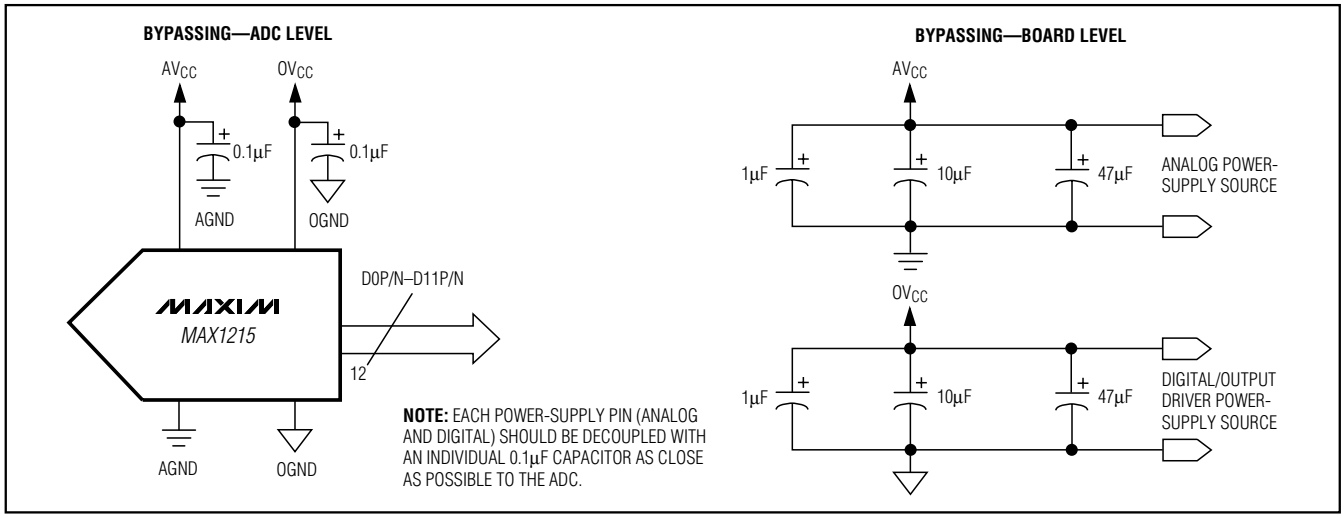


Figure 10. Grounding, Bypassing, and Decoupling Recommendations for the MAX1215

Static Parameter Definitions

Integral Nonlinearity (INL)

Integral nonlinearity is the deviation of the values on an actual transfer function from a straight line. This straight line can be either a best straight-line fit or a line drawn between the end points of the transfer function, once offset and gain errors have been nullified. However, the static linearity parameters for the MAX1215 are measured using the histogram method with a 10MHz input frequency.

Differential Nonlinearity (DNL)

Differential nonlinearity is the difference between an actual step width and the ideal value of 1LSB. A DNL error specification of less than 1LSB guarantees no missing codes and a monotonic transfer function. The MAX1215's DNL specification is measured with the histogram method based on a 10MHz input tone.

Dynamic Parameter Definitions

Aperture Jitter

Figure 11 depicts the aperture jitter (t_{AJ}), which is the sample-to-sample variation in the aperture delay.

Aperture Delay

Aperture delay (t_{AD}) is the time defined between the rising edge of the sampling clock and the instant when an actual sample is taken (Figure 11).

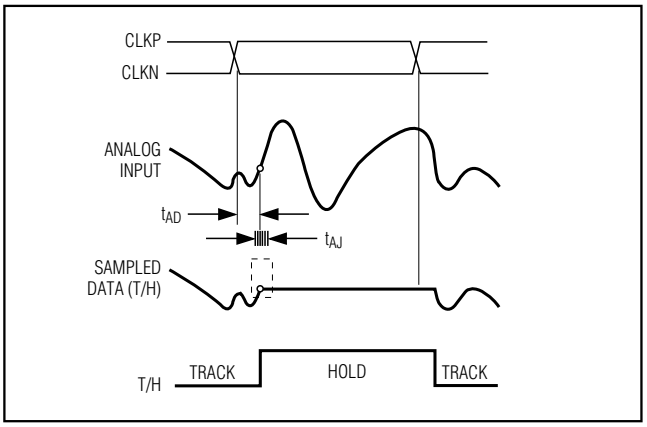


Figure 11. Aperture Jitter/Delay Specifications

Signal-to-Noise Ratio (SNR)

For a waveform perfectly reconstructed from digital samples, the theoretical maximum SNR is the ratio of the full-scale analog input (RMS value) to the RMS quantization error (residual error). The ideal, theoretical minimum analog-to-digital noise is caused by quantization error only and results directly from the ADC's resolution (N bits):

$$SNR_{[max]} = 6.02 \times N + 1.76$$

In reality, other noise sources such as thermal noise, clock jitter, signal phase noise, and transfer function nonlinearities are also contributing to the SNR calculation and should be considered when determining the signal-to-noise ratio in ADC.

Signal-to-Noise Plus Distortion (SINAD)

SINAD is computed by taking the ratio of the RMS signal to all spectral components excluding the fundamental and the DC offset. In the case of the MAX1215, SINAD is computed from a curve fit.

Spurious-Free Dynamic Range (SFDR)

SFDR is the ratio of RMS amplitude of the carrier frequency (maximum signal component) to the RMS value of the next-largest noise or harmonic distortion component. SFDR is usually measured in dBc with respect to the carrier frequency amplitude or in dBFS with respect to the ADC's full-scale range.

Intermodulation Distortion (IMD)

IMD is the ratio of the RMS sum of the intermodulation products to the RMS sum of the two fundamental input tones. This is expressed as:

$$IMD = 20 \times \log\left(\frac{\sqrt{V_{IM1}^2 + V_{IM2}^2 + ... + V_{IM3}^2 + V_{IMn}^2}}{\sqrt{V_1^2 + V_2^2}}\right)$$

The fundamental input tone amplitudes (V_1 and V_2) are at -7dBFS. The intermodulation products are the amplitudes of the output spectrum at the following frequencies:

- Second-order intermodulation products: $f_{IN1} + f_{IN2}$, $f_{IN2} - f_{IN1}$
- Third-order intermodulation products: $2 \times f_{IN1} - f_{IN2}$, $2 \times f_{IN2} - f_{IN1}$, $2 \times f_{IN1} + f_{IN2}$, $2 \times f_{IN2} + f_{IN1}$
- Fourth-order intermodulation products: $3 \times f_{IN1} - f_{IN2}$, $3 \times f_{IN2} - f_{IN1}$, $3 \times f_{IN1} + f_{IN2}$, $3 \times f_{IN2} + f_{IN1}$
- Fifth-order intermodulation products: $3 \times f_{IN1} - 2 \times f_{IN2}$, $3 \times f_{IN2} - 2 \times f_{IN1}$, $3 \times f_{IN1} + 2 \times f_{IN2}$, $3 \times f_{IN2} + 2 \times f_{IN1}$

Full-Power Bandwidth

A large -1dBFS analog input signal is applied to an ADC and the input frequency is swept up to the point where the amplitude of the digitized conversion result has decreased by 3dB. The -3dB point is defined as the full-power input bandwidth frequency of the ADC.

1.8V, 12-Bit, 250Msps ADC for Broadband Applications

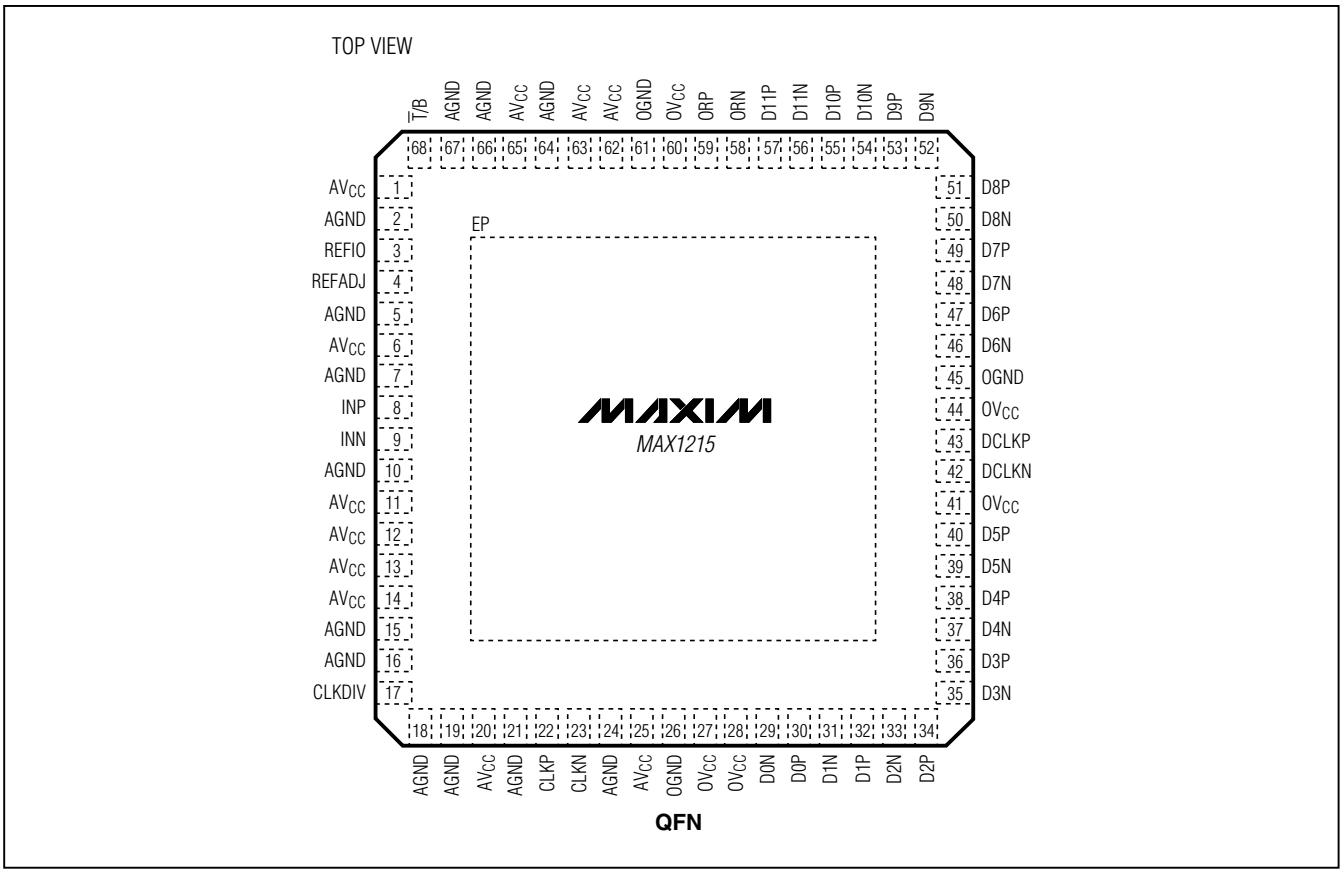
Noise-Power Ratio (NPR)

NPR is commonly used to characterize the return path of cable systems where the signals are typically individual quadrature amplitude-modulated (QAM) carriers with a frequency spectrum similar to noise. Numerous such carriers are operated in a continuous spectrum, generating a noise-like signal, which covers a relatively broad bandwidth. To test the MAX1215 for NPR, a "noise-like" signal is passed through a high-order bandpass filter to produce an approximately square spectral pedestal of noise with about the same bandwidth as the signals being simulated. Following the bandpass filter, the signal is passed through a narrow band-reject filter to produce a deep notch at the center of the noise pedestal. Finally, this signal is applied to the MAX1215 and its digitized results analyzed. The RMS noise power of the signal inside the notch is compared with the RMS noise level outside the notch using an FFT. Note that the NPR test requires sufficiently long data records to guarantee a suitable number of samples inside the notch. NPR for the MAX1215 was determined for 50MHz noise bandwidth signals, simulating a typical cable signal environment (see the *Typical Operating Characteristics* for test details and results), and with a notch frequency of 28.8MHz.

Pin-Compatible, Lower-Speed/Resolution Versions

Applications that require lower resolution and/or higher speed can refer to other family members of the MAX1215. Adjusting an application to a lower resolution has been simplified by maintaining an identical pinout for all members of this high-speed family. See the *Pin-Compatible Versions* table on the first page of this data sheet for a selection of different resolution and speed grades.

Pin Configuration

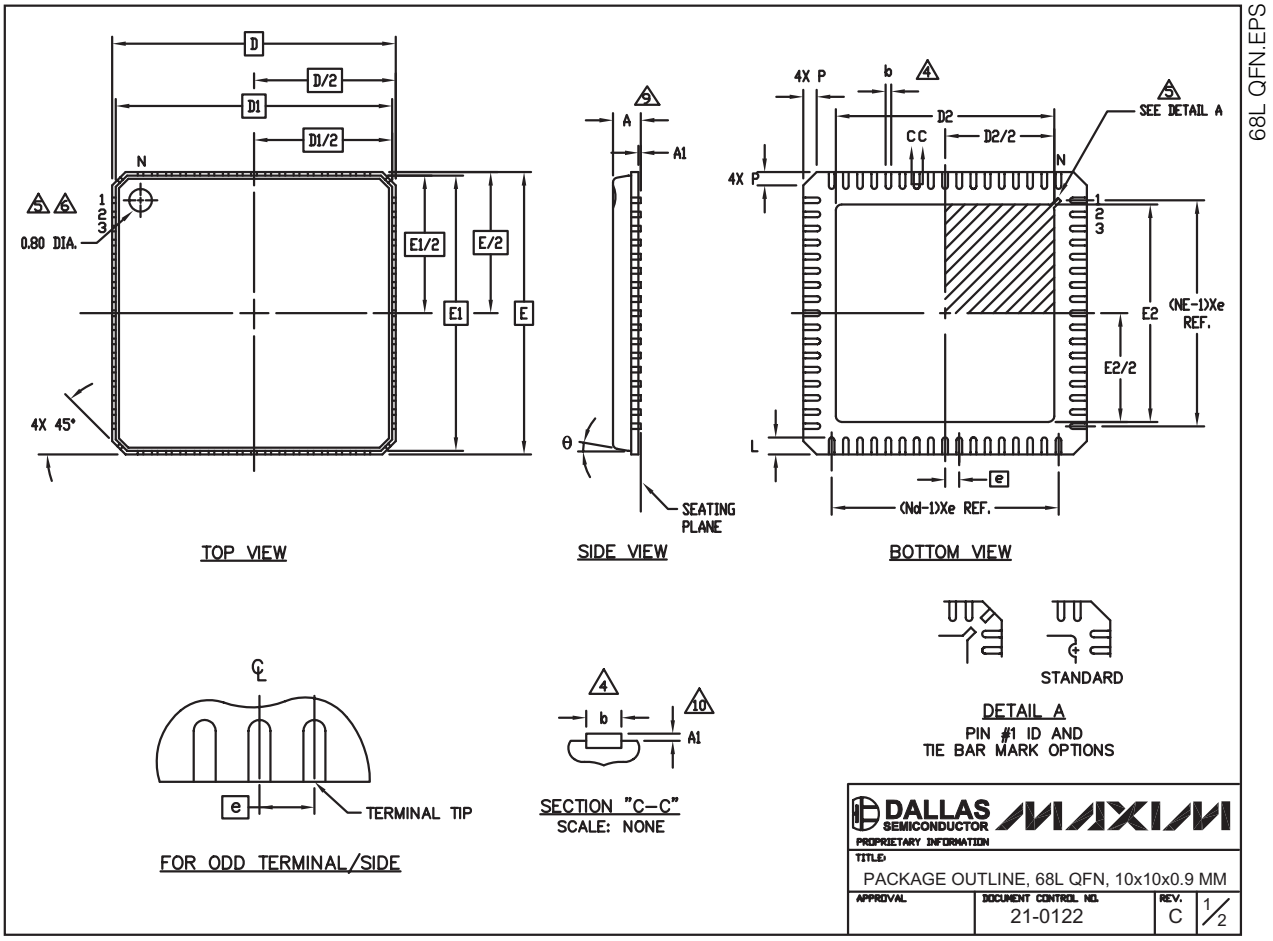


1.8V, 12-Bit, 250Msps ADC for Broadband Applications

Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to **www.maxim-ic.com/packages**.)

For the MAX1215 , the package code is G6800-4.



1.8V, 12-Bit, 250Msps ADC for Broadband Applications

Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to **www.maxim-ic.com/packages**.)

SYMBOL	COMMON DIMENSIONS			NOTE
	MIN.	NOM.	MAX.	
A	–	0.90	1.00	
A1	0.00	0.01	0.05	11
b	0.18	0.23	0.30	4
D		10.00 BSC		
D1		9.75 BSC		
e		0.50 BSC		
E		10.00 BSC		
E1		9.75 BSC		
L	0.50	0.60	0.65	
N		68		3
Nd		17		3
Ne		17		3
θ	0		12°	
P	0	0.42	0.60	

1. DIE THICKNESS ALLOWABLE IS .012 INCHES MAXIMUM.
2. DIMENSIONING & TOLERANCES CONFORM TO ASME Y14.5M. – 1994.
3. N IS THE NUMBER OF TERMINALS.
   Nd IS THE NUMBER OF TERMINALS IN X–DIRECTION &
   Ne IS THE NUMBER OF TERMINALS IN Y–DIRECTION.
4. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.20 AND 0.25mm FROM TERMINAL TIP.
5. THE PIN #1 IDENTIFIER MUST BE LOCATED ON THE TOP SURFACE OF THE PACKAGE BY USING INDENTATION MARK OR OTHER FEATURE OF PACKAGE BODY. DETAILS OF PIN #1 IDENTIFIER IS OPTIONAL, BUT MUST BE LOCATED WITHIN ZONE INDICATED.
6. EXACT SHAPE AND SIZE OF THIS FEATURE IS OPTIONAL.
7. ALL DIMENSIONS ARE IN MILLIMETERS.
8. PACKAGE WARPAGE MAX 0.10mm.
9. APPLIES TO EXPOSED SURFACE OF PADS AND TERMINALS
10. APPLIES ONLY TO TERMINALS.
11. MEETS JEDEC MO–220.

EXPOSED PAD VARIATIONS						
	D2			E2		
PKG CODE	MIN	NOM	MAX	MIN	NOM	MAX
G6800-2	7.55	7.70	7.85	7.55	7.70	7.85
G6800-4	5.65	5.80	5.95	5.65	5.80	5.95

DALLAS SEMICONDUCTOR MAXIM
PROPRIETARY INFORMATION

TITLE: PACKAGE OUTLINE, 68L QFN, 10x10x0.9 MM

APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-0122	C	1/2